UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,549	04/02/2001	Yoshimitsu Nakashima	70840-55652	9425

21874 7590 04/21/2004

EDWARDS & ANGELL, LLP
P.O. BOX 55874
BOSTON, MA 02205

EXAMINER	
HARRINGTON, ALICIA M	
ART UNIT	**PAPER NUMBER**
2873	

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,549	NAKASHIMA, YOSHIMITSU	
	Examiner	Art Unit	
	Alicia M Harrington	2873	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE and amendment filed on 2/2/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6* is/are allowed.

6)☒ Claim(s) *1-5 and 7-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/2/04 has been entered.

Claim Objections

2. Claim 5 is objected to because of the following informalities: In line 14, the Examiner believes a coma between the words passivation and section should be omitted.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 8-11, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants admitted prior art (figure 5A-5B pages 2-7) in view of Lin et al US 6, 396,089).

Regarding claims 1,3,4,9,10 applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14); a light reception section (12); passivation section (15) with a refractive index (2.0; see page 6) and overlying the light shield section, light reception sections and aperture; a planarization section (16) overlying the passivation section, where the planarization section has a refractive index (1.5 ort 1.6; see page 6) smaller than the refractive index of the passivation section. However, applicant admitted prior art fails to discloses a planar /flat top surface for the passivation section. Although, it is well known in the art, as taught by Lin.

In the same field of endeavor, Lin discloses the planarization of semiconductor device where the passivation layer with SOG film that (304,306,308,310) is planarized (col. 3, lines 22-65). The passivation films have several layers that are placed over light reception area. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify, applicant's admitted prior art, as taught by Lin, to provide superior insulating property.

Regarding claim 2, applicant discloses the passivation film is made of silicon nitride based film (see pages 2-4).

Regarding claim 8, applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14); a light reception section (12); passivation section (15) film (n=2) overlying the light shield section, light reception sections and aperture; a planarization section (16) overlying the passivation section, where the planarization section has a refractive index (n=1.5 or 1.6; see page 6) smaller than the refractive index of the passivation section. However, applicant admitted prior art

fails to discloses a planar /flat top surface for the passivation section, chemical machine polishing and insulation section. Although, it is well known in the art, as taught by Lin.

In the same field of endeavor, Lin discloses a method for manufacturing a semiconductor image sensor where the passivation film is planarized and where in the method comprises applying an SOG film and a forming another film over the SOG for forming the passivation section (col. 3, lines 22-65) to produce a substantial planarized surface. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify applicant's admitted prior art, as taught by Lin, since it would provide a planarized passivation layer which contributes to protection of the circuit and performance.

Regarding claim 13, applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14); a light reception section (12); passivation section (15) film overlying the light shield section, light reception sections and aperture where the passivation provides moisture and chemical resistance (see page 3). However, applicant admitted prior art fails to discloses a planar /flat top surface. Although, it is well known in the art, as taught by Lin.

In the same field of endeavor, Lin discloses the planarization of semiconductor device where the passivation layer with SOG film that (304,306,308,310) is planarized (col. 3, lines 22-65) Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify, applicant's admitted prior art, as taught by Lin et al. to provide a planar surface which enhances image quality and provides protection for the detector.

5. Claims 5,7,11,12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants admitted prior art (figure 5A-5B pages 2-7) in view of Lin et al US 6, 396,089), further in view of De Santi et al (EP 0887 847 A1).

Regarding claims 5 and 11, applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14); a light reception section (12); passivation section (15; n=2) film overlying the light shield section, light reception sections and aperture; a planarization section (16) overlying the passivation section, where the planarization section has a refractive index (n=1.5 ort 1.6; see page 6) smaller than the refractive index of the passivation section. However, applicant admitted prior art fails to discloses a planar /flat top surface for the passivation section and chemical machine polishing as claimed. Although, it is well known in the art, as taught by Lin.

In the same field of endeavor, Lin discloses the planarization of semiconductor device where the passivation layer with SOG film that (304,306,308,310) is planarized (col. 3, lines 22-65). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify, applicant's admitted prior art, as taught Lin et al. to provide a planar surface which enhances image quality and provides protection for the detector.

In addition, the application and Lin discloses applying the thin film forming the passivation section by using a CVD technique or the like. Although, applicant and Lin fail to produce a planarized layer using chemical mechanical polishing, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify applicant and Lin, to include this process since it is a notoriously well known

semiconductor planarization layering process, as taught by De Santi (EP 0887,847) in col. 3,lines 35-36.

Regarding claims 7 and 12, applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14); a light reception section (12); passivation section (15) film overlying the light shield section, light reception sections and aperture where the passivation provides moisture and chemical resistance (see page 3); a planarization section (16;n=2) overlying the passivation section, where the planarization section has a refractive index (n=1.5 ort 1.6; see page 6) smaller than the refractive index of the passivation section. However, applicant admitted prior art fails to disclose a planar /flat top surface for the passivation section, an insulation layer and chemical machine polishing as claimed. Although, it is well known in the art, as taught by Lin.

In the same field of endeavor, Lin discloses the planarization of semiconductor device where the passivation layer with SOG film that (304,306,308,310) is planarized (col. 3, lines 22-65). The passivation films have several layers that are placed over light reception area. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify, applicant's admitted prior art, as taught by Lin, to provide superior insulating property.

In addition, the application and Lin discloses applying the thin film forming the passivation section by using a CVD technique or the like. Although, applicant and Lin fail to produce a planarized layer using chemical mechanical polishing, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify applicant and park, to include this process since it is a notoriously well known

semiconductor planarization layering process, as taught by De Santi (EP 0887,847) in col. 3,lines 35-36.

Regarding claim 14, applicant's admitted prior art discloses a solid state imaging device comprising a semiconductor (11), light shield (14); a light reception section (12); passivation section (15) film overlying the light shield section, light reception sections and aperture. However, applicant admitted prior art fails to discloses a planar /flat top surface. Although, it is well known in the art, as taught by Lin.

In the same field of endeavor, Lin discloses the planarization of semiconductor device where the passivation layer with SOG film that (304,306,308,310) is planarized (col. 3, lines 22-65) Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify, applicant's admitted prior art, as taught by Lin et al. to provide a planar surface which enhances image quality and provides protection for the detector.

In addition, the application and Lin discloses applying the thin film forming the passivation section by using a CVD technique or the like. Although, applicant and Lin fail to produce a planarized layer using chemical mechanical polishing, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify applicant and Lin, to include this process since it is a notoriously well known semiconductor planarization layering process, as taught by De Santi (EP 0887,847) in col. 3,lines 35-36.

Response to Arguments

6. Applicant's arguments with respect to claims 1-5,7-14 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

7. Claim 6 is allowed.

The following is a statement of reasons for the indication of allowable subject matter: Regarding claim 6, prior art taken either singularly or in combination fails to anticipate or fairly suggest the limitations of the dependent claims, in such manner that a rejection under 35 U.S.C 102 or 103 would be proper. The prior art fails to teach a combination of all the claimed features as presented in independent claims, which include a method for producing a solid state imaging device where flattening of the passivation section is performed under the condition that a selective ration of 1:1 implemented as claimed.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alicia M Harrington whose telephone number is 571 272 2330. The examiner can normally be reached on Monday - Thursday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on 571 272 2328. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alicia M Harrington
Examiner
Art Unit 2873

AMH

Georgia Epps
Supervisory Patent
Technology Cen